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09/843,198

Main Menu | Search Form | Posting Counts | Show S Numbers | Edit S Numbers | Preferences | Cases

Search Results -

Terms	Documents
L5 and (resist near5 patterning)	3

Database: US Patents Full-Text Database; US Pre-Grant Publication Full-Text Database; JPO Abstracts Database; EPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Search: L6

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Search History

DATE: Sunday, September 15, 2002 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=YES; OP=OR			
L6	L5 and (resist near5 patterning)	3	L6
L5	L4 and (copper near2 plating)	65	L5
L4	L1 and cmp	202	L4
L3	L1 and (cmp or (chemical mechanical polishing))	459	L3
L2	L1 and cmp or (chemical mechanical polishing)	1079242	L2
L1	copper adj seed	500	L1

END OF SEARCH HISTORY

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Search Results - Record(s) 1 through 3 of 3 returned.

☐ 1. Document ID: US 6350688 B1

L6: Entry 1 of 3 File: USPT Feb 26, 2002

US-PAT-NO: 6350688
DOCUMENT-IDENTIFIER: US 6350688 B1

TITLE: Via RC improvement for copper damascene and beyond technology

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw. Desc | Image

☐ 2. Document ID: US 6225226 B1

L6: Entry 2 of 3 File: USPT May 1, 2001

US-PAT-NO: 6225226
DOCUMENT-IDENTIFIER: US 6225226 B1

TITLE: Method for processing and integrating copper interconnects

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw. Desc | Image

☐ 3. Document ID: US 6184138 B1

L6: Entry 3 of 3 File: USPT Feb 6, 2001

US-PAT-NO: 6184138
DOCUMENT-IDENTIFIER: US 6184138 B1

TITLE: Method to create a controllable and reproducible dual copper damascene structure

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw. Desc | Image

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Terms	Documents
L5 and (resist near5 patterning)	3

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Search Results -

Terms	Documents
L10 and (diffusion near barrier)	3

Database: US Patents Full-Text Database
US Pre-Grant Publication Full-Text Database
JPO Abstracts Database
EPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L11

Refine Search

Recall Text | Clear

Search History

DATE: Sunday, September 15, 2002 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
	DB=USPT; PLUR=YES; OP=OR		
L11	L10 and (diffusion near barrier)	3	L11
L10	L9 and patterning	7	L10
L9	L8 and plating	9	L9
L8	L4 and (developing near5 (resist or photoresist))	13	L8
L7	L4 and (trimming near5 resist)	0	L7
L6	L5 and (resist near5 patterning)	3	L6
L5	L4 and (copper near2 plating)	65	L5
L4	L1 and cmp	202	L4
L3	L1 and (cmp or (chemical mechanical polishing))	459	L3
L2	L1 and cmp or (chemical mechanical polishing)	1079242	L2
L1	copper adj seed	500	L1

END OF SEARCH HISTORY

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Search Results - Record(s) 1 through 7 of 7 returned.

1. Document ID: US 6433432 B1

L10: Entry 1 of 7 File: USPT Aug 13, 2002

US-PAT-NO: 6433432
DOCUMENT-IDENTIFIER: US 6433432 B1

TITLE: Semiconductor device having fluorined insulating film and reduced fluorine at interconnection interfaces and method of manufacturing the same

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw. Desc | Image

2. Document ID: US 6420261 B2

L10: Entry 2 of 7 File: USPT Jul 16, 2002

US-PAT-NO: 6420261
DOCUMENT-IDENTIFIER: US 6420261 B2

TITLE: Semiconductor device manufacturing method

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw. Desc | Image

3. Document ID: US 6280640 B1

L10: Entry 3 of 7 File: USPT Aug 28, 2001

US-PAT-NO: 6280640
DOCUMENT-IDENTIFIER: US 6280640 B1

TITLE: Process for manufacturing a chip carrier substrate

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw. Desc | Image

4. Document ID: US 6262376 B1

L10: Entry 4 of 7 File: USPT Jul 17, 2001

US-PAT-NO: 6262376
DOCUMENT-IDENTIFIER: US 6262376 B1

TITLE: Chip carrier substrate

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw. Desc | Image

☐ 5. Document ID: US 6110819 A

L10: Entry 5 of 7 File: USPT Aug 29, 2000

US-PAT-NO: 6110819
DOCUMENT-IDENTIFIER: US 6110819 A

TITLE: Interconnect structure using Al.sub.2 Cu for an integrated circuit chip

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw. Desc | Image

☐ 6. Document ID: US 5925933 A

L10: Entry 6 of 7 File: USPT Jul 20, 1999

US-PAT-NO: 5925933
DOCUMENT-IDENTIFIER: US 5925933 A

TITLE: Interconnect structure using Al.sub.2 -Cu for an integrated circuit chip

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw. Desc | Image

☐ 7. Document ID: US 5565707 A

L10: Entry 7 of 7 File: USPT Oct 15, 1996

US-PAT-NO: 5565707
DOCUMENT-IDENTIFIER: US 5565707 A

TITLE: Interconnect structure using a Al.sub.2 Cu for an integrated circuit chip

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw. Desc | Image

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Terms	Documents
L9 and patterning	7

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Search Results - Record(s) 1 through 3 of 3 returned.

1. Document ID: US 6110819 A

L11: Entry 1 of 3 File: USPT Aug 29, 2000

US-PAT-NO: 6110819
DOCUMENT-IDENTIFIER: US 6110819 A

TITLE: Interconnect structure using Al.sub.2 Cu for an integrated circuit chip

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw Desc | Image

2. Document ID: US 5925933 A

L11: Entry 2 of 3 File: USPT Jul 20, 1999

US-PAT-NO: 5925933
DOCUMENT-IDENTIFIER: US 5925933 A

TITLE: Interconnect structure using Al.sub.2 -Cu for an integrated circuit chip

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw Desc | Image

3. Document ID: US 5565707 A

L11: Entry 3 of 3 File: USPT Oct 15, 1996

US-PAT-NO: 5565707
DOCUMENT-IDENTIFIER: US 5565707 A

TITLE: Interconnect structure using a Al.sub.2 Cu for an integrated circuit chip

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw Desc | Image

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Terms	Documents
L10 and (diffusion near barrier)	3

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